CT2 Front End IC

Chip Specification

Description

U7001BG is a monolithic GaAs transmit/ receive front end with power amplifier, low noise amplifier and antenna switch. It is specially designed for operation in CT2 band and suitable for a frequency range of 839 MHz to 952 MHz with external matching.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Low supply voltage 3.6 V typical (min. 2.7 V)
- High power added efficiency (typ. 40%)
- Low power consumption in receive mode
- Power down control pin for low noise amplifier
- Gain control of power amplifier
- Low noise amplifier
- Optional high output power 50 mW @ 5 V supply voltage

Benefits

- Extended talk time due to low power consumption and high PAE
- Few external components needed

Block Diagram

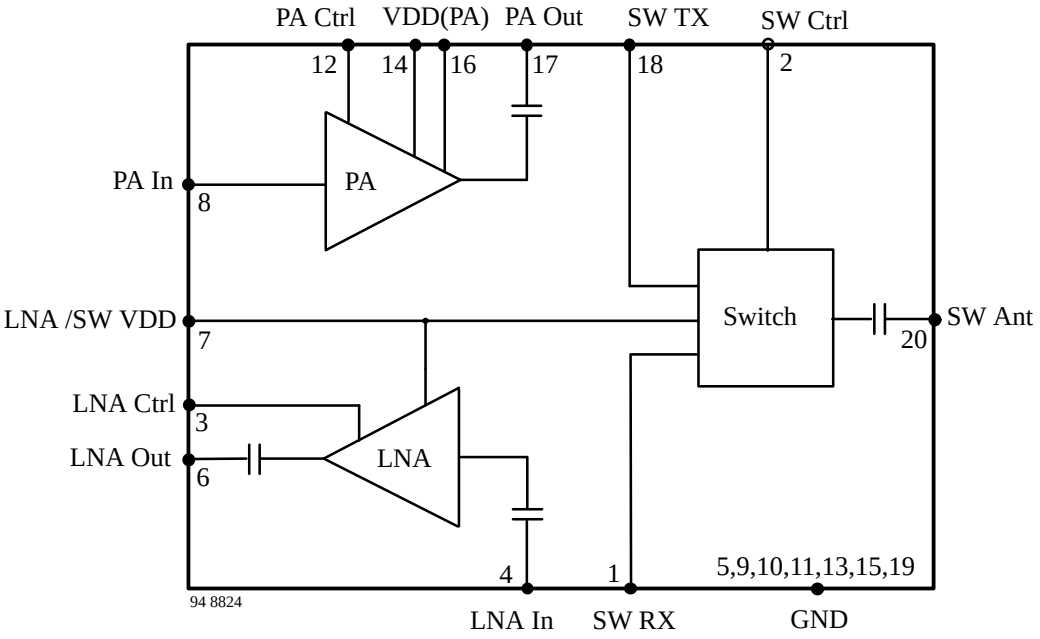

Figure 1. Block diagram

Pad Description

* to be supplemented later

Pad	Symbol	Function
tbd	SW RX	Switch RX output
tbd	SW Ctrl	Switch control input
tbd	LNA Ctrl	LNA control input
tbd	LNA In	Low noise amplifier input
tbd	GND	Ground
tbd	LNA Out	LNA output
tbd	LNA/SW VDD	LNA & Switch power supply voltage
tbd	PA In	Power amplifier input
tbd	PA Ctrl	PA control input
tbd	PA VDD1	PA power supply voltage 1
tbd	PA VDD2	PA power supply voltage 2
tbd	PA Out	PA output
tbd	SW TX	Switch TX input
tbd	SW Ant	Switch antenna output

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltages	Pins 7, 14 and 16	VDD	+ 7	V
Input voltages	Pins 4, 8, 18 and 20	V_i	0 to VDD	V
Control voltages	Pins 2, 3 and 12	V_C	0 to VDD	V
Channel temperature		T_{ch}	125	°C
Storage temperature range		T_{stg}	– 40 to + 125	°C

Operating Range

Parameters		Symbol	Value	Unit
Supply voltage	Pin 7	LNA/SW VDD	2.7 to 5.25	V
Supply voltage	Pins 14 and 16	VDD	2.7 to 5.25	V
Ambient temperature range		T_{amb}	– 40 to + 85	°C

Electrical Characteristics Low Noise Amplifier (LNA)

Test conditions (unless otherwise specified): **VDD = 3.3 V**, T_{amb} = 25°C, referred to test circuit.
System impedance Zo = 50 Ω, f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 7	VDD	2.7	3.6	5.25	V
Supply current	@ VDD = 3.3 V, Pin 7	Is		7	8	mA
Supply current	@ VDD = 3.3 V, Pin 7; LNA Ctrl = 0 V: LNA“off”	Is		0.3	0.5	mA
Frequency range	Pin 4	f	839	866	952	MHz
Linear power gain	Pins 4 and 6	Gp	16	18		dB
Noise figure	Pins 4 and 6	NF		1.8	2.0	dB
Compression	Pins 4 and 6	P_1dB	– 29	– 27		dBm
Third order input intercept point	Pins 4 and 6	IIP3	– 19	– 17		dBm
Isolation	Pins 6 and 4 (from output to input)	$Isol_{LNA}$	23	28		dB
Input impedance	Pin 4			50		Ω
Output impedance	Pin 6		50	100		Ω
LNA control voltage	Pin 3: LNA Mode “off” Pin 3: LNA Mode “on”	LNA Ctrl	 VDD–0.5	0.0 VDD	0.5	V

Test conditions (unless otherwise specified); **VDD = 2.7 V**, T_{amb} = 25°C, referred to test circuit.
System impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 7	VDD	2.7	3.6	5.25	V
Supply current	@ VDD = 2.7 V, Pin 7	Is		6	7	mA
Supply current	@ VDD = 2.7 V, Pin 7; LNA Ctrl = 0 V: LNA“off”	Is		0.25	0.5	mA
Frequency range	Pin 4	f	839	866	952	MHz
Linear power gain	Pins 4 and 6	Gp	15	17		dB
Noise figure	Pins 4 and 6	NF		1.8	2.0	dB
Compression	Pins 4 and 6	P_1dB	– 29	– 28		dBm
Third order input intercept point	Pins 4 and 6	IIP3	– 19	– 18		dBm
Isolation	Pins 6 and 4 (from output to input)	$Isol_{LNA}$	23	28		dB
Input impedance	Pin 4			50		Ω
Output impedance	Pin 6		50	100		Ω
LNA control voltage	Pin 3: LNA Mode “off” Pin 3: LNA Mode “on”	LNA Ctrl	 VDD–0.5	0.0 VDD	0.5	V

Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified); **VDD = 5.0 V**, PA Ctrl = 5 V, Tamb = 25°C, referred to test circuit.
System Impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pins 14 and 16	VDD1,2	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	Is		32	36	mA
Supply current	Pin 12	I Ctrl		2.5	3.0	mA
Supply current in power down mode	Pins 14 and 16; @ Pin 12 = 0.0 V PA "off"	Is			50	µA
Frequency range	Pin 8	f	839	866	952	MHz
Linear power gain	Pins 8 and 17	Gp	35	37	tbd.	dB
Power response	@ P_{in} = – 15 dBm					
Output Power	At 3 dB gain compression; Pin 17	P_{out}	17*	19*		dBm
Gain control range	Pins 17 and 12	G_c	35	37		dB
Gain control voltage	Pout = $Pout_{max}$	PA Ctrl		4.5	VDD	V
Gain control voltage	Pout = $Pout_{max – 16 dB}$	PA Ctrl	1		1.8	V
Gain control voltage	Pout = $Pout_{min}$	PA Ctrl		0.0		V
Switching time	Pins 12 and 17					
Turn on time	90% $Pout_{max}$	t_{on}			2	µs
Turn off time	10% $Pout_{max}$	t_{off}			5	µs
Harmonic levels	At 3 dB gain compression		– 18	– 25		dBc
Isolation	Pins 17 and 8 (from output to input)	$Isol_{PA}$	23	28		dB
Input matching	Pin 8	$VSWR_{in}$	1.9 : 1	1.6 : 1		
Output matching	Pin 17	$VSWR_{out}$		2.0 : 1		
Power added efficiency	Pin 17	η_{PAE}	35	40		%
Input impedance	Pin 8	Z_{in}		50		Ω
Output impedance	Pin 17	Z_{out}		50		Ω

* Optional 2 dB higher with one mask level modified

Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified); **VDD = 3.6 V**, PA Ctrl = 3.6 V, Tamb = 25°C, referred to test circuit.
System impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pins 14 and 16	VDD1,2	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	Is		28	33	mA
Supply current	Pin 12	I Ctrl		2.0	2.5	mA
Supply current in power down mode	Pins 14 and 16; @ Pin 12 = 0.0 V PA “off”	Is			50	µA
Frequency range	Pin 8	f	839	866	952	MHz
Linear power gain	Pins 8 and 17	Gp	33	35	tbd.	dB
Power response	@ P_{in} = – 15 dBm					
Output Power	At 3 dB gain compression; Pin 17	P_{out}	15*	17*	tbd.	dBm
Gain control range	Pins 17 and 12	G_c	33	35		dB
Gain control voltage	Pout = $Pout_{max}$	PA Ctrl		2.9	VDD	V
Gain control voltage	Pout = $Pout_{max – 16 dB}$	PA Ctrl	0.9		1.7	V
Gain control voltage	Pout = $Pout_{min}$	PA Ctrl		0.0		V
Switching time	Pins 12 and 17					
Turn on time	90% $Pout_{max}$	t_{on}			2	µs
Turn off time	10% $Pout_{max}$	t_{off}			5	µs
Harmonic levels	At 3 dB gain compression		– 18	– 25		dBc
Isolation	Pins 17 and 8 (from output to input)	$Isol_{PA}$	23	28		dB
Input matching	Pin 8	$VSWR_{in}$	1.9 : 1	1.6 : 1		
Output matching	Pin 17	$VSWR_{out}$		2.0 : 1		
Power added efficiency	Pin 17	η_{PAE}	40	46		%
Input impedance	Pin 8	Z_{in}		50		Ω
Output impedance	Pin 17	Z_{out}		50		Ω

* Optional 2 dB higher with one mask level modified

Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified); **VDD = 2.7 V**, PA Ctrl = 2.7 V, T_{amb} = 25°C, referred to test circuit. System impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pins 14 and 16	VDD1,2	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	Is		24	28.5	mA
Supply current	Pin 12	I Ctrl		2.0	2.5	mA
Supply current in power down mode	Pins 14 and 16; @ Pin 12 = 0.0 V PA "off"	Is			50	µA
Frequency range	Pin 8	f	839	866	952	MHz
Linear power gain	Pins 8 and 17	Gp	32	34	tbd.	dB
Power response	@ P_{in} = –15 dBm					
Output Power	At 3 dB gain compression; Pin 17	P_{out}	14*	16*	tbd.	dBm
Gain control range	Pins 17 and 12	G_c	32	34		dB
Gain control voltage	Pout = $Pout_{max}$	PA Ctrl		2.5	VDD	V
Gain control voltage	Pout = $Pout_{max – 16 dB}$	PA Ctrl	0.9		1.7	V
Gain control voltage	Pout = $Pout_{min}$	PA Ctrl		0.0		V
Switching time	Pins 12 and 17					
Turn on time	90% $Pout_{max}$	t_{on}		2		µs
Turn off time	10% $Pout_{max}$	t_{off}		5		µs
Harmonic levels	At 3 dB gain compression		– 20	– 25		dBc
Isolation	Pins 16, 8 (from output to input)	$Isol_{PA}$	23	28		dB
Input matching	Pin 8	$VSWR_{in}$	1.9 : 1	1.4 : 1		
Output matching	Pin 16	VSWRout		2.0 : 1		
Power added efficiency	Pin 16	η_{PAE}	35	40		%
Input impedance	Pin 8	Z_{in}		50		Ω
Output impedance	Pin 16	Z_{out}		50		Ω

* Optional 2 dB higher with one mask level modified

Electrical Characteristics Antenna Switch

Test conditions (unless otherwise specified); **VDD = 3.6 V**, Tamb = 25°C, referred to test circuit.
System impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 7	LNA/SW VDD	2.7	3.6	5.0	V
Frequency range	Pins 1, 18 and 20	f	839	866	952	MHz
Insertion loss	@ P_{in} = +17 dBm; Pin 18 to Pin 20; "TX Mode"	IL_{TX}		0.5	0.8	dB
Isolation	@ P_{in} = +17 dBm; Pin 18 to Pin 1; "TX Mode"	$Isol_{TX}$	16	18		dB
Insertion loss	@ P_{in} = –26 dBm; Pin 20 to Pin 1; "RX Mode"	IL_{RX}		0.5	0.8	dB
Isolation	@ P_{in} = –26 dBm; Pin 20 to Pin 18; "RX Mode"	$Isol_{TX}$	16	18		dB
Switch control	RX Mode; Pin 2	SW Ctrl	0	0	0.3	V
	TX Mode	SW Ctrl	VDD –0.5	VDD	VDD +0.5	V
Input impedance	TX Mode; Pin 18	Z_{in}		50		Ω
"	RX Mode; Pin 1	Z_{in}		50		Ω
Output impedance	RX TX–Mode; Pin 20	Z_{out}		50		Ω

Test conditions (unless otherwise specified); **VDD = 2.7 V**, Tamb = 25°C, referred to test circuit.
System impedance Zo = 50 Ω; f_{RF} = 866 MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 7	LNA/SW VDD	2.7	3.6	5.0	V
Frequency range	Pins 1, 18 and 20	f	839	866	952	MHz
Insertion loss	@ P_{in} = +15 dBm; Pin 18 to Pin 20; "TX Mode"	IL_{TX}		0.5	0.8	dB
Isolation	@ P_{in} = +15 dBm; Pin 18 to Pin 1; "TX Mode"	$Isol_{TX}$	16	18		dB
Insertion loss	@ P_{in} = –26 dBm; Pin 20 to Pin 1; "RX Mode"	IL_{RX}		0.5	0.8	dB
Isolation	@ P_{in} = –26 dBm; Pin 20 to Pin 18; "RX–Mode"	$Isol_{TX}$	16	18		dB
Switch control	RX Mode; Pin 2	SW Ctrl	0	0	0.3	V
	TX Mode; Pin 2	SW Ctrl	VDD –0.5	VDD	VDD +0.5	V
Input impedance	TX Mode; Pin 18	Z_{in}		50		Ω
Input impedance	RX Mode; Pin 1	Z_{in}		50		Ω
Output impedance	RX TX–Mode; Pin 20	Z_{out}		50		Ω

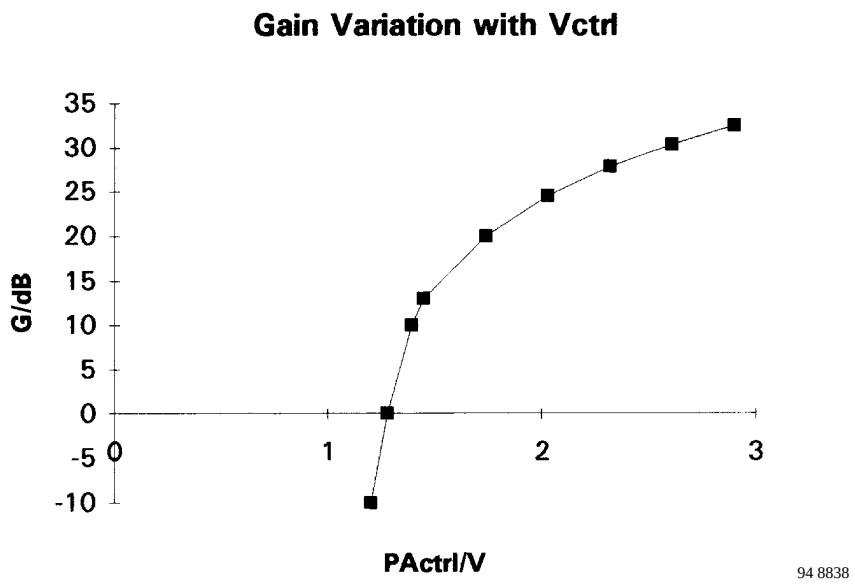

Figure 2. Gain variation of power amplifier with switch and filter. @ VDD = 3.6 V (typical values)

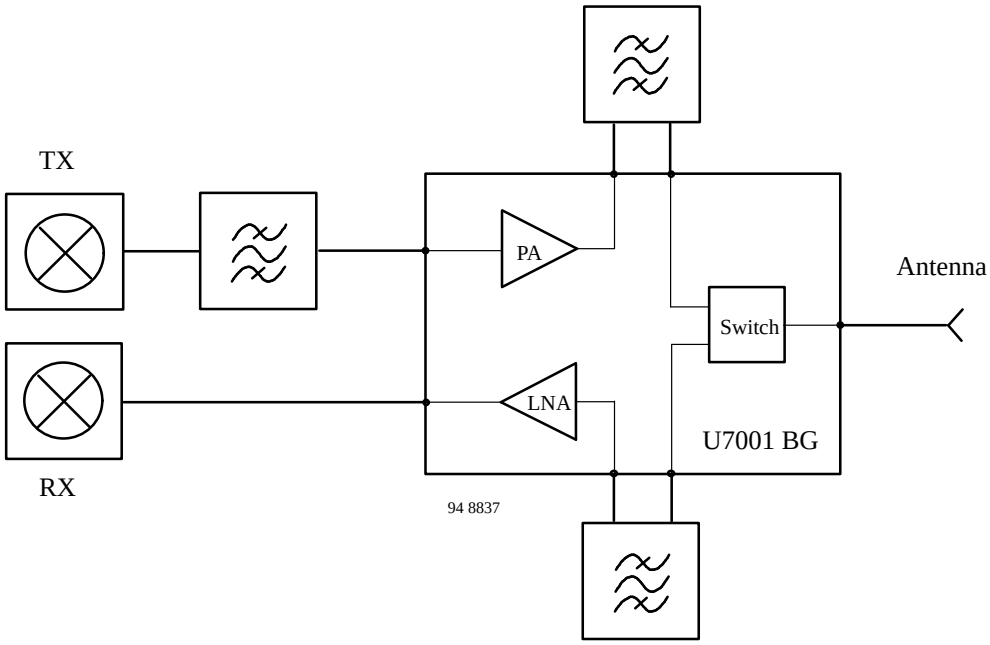

Figure 3. Application 1

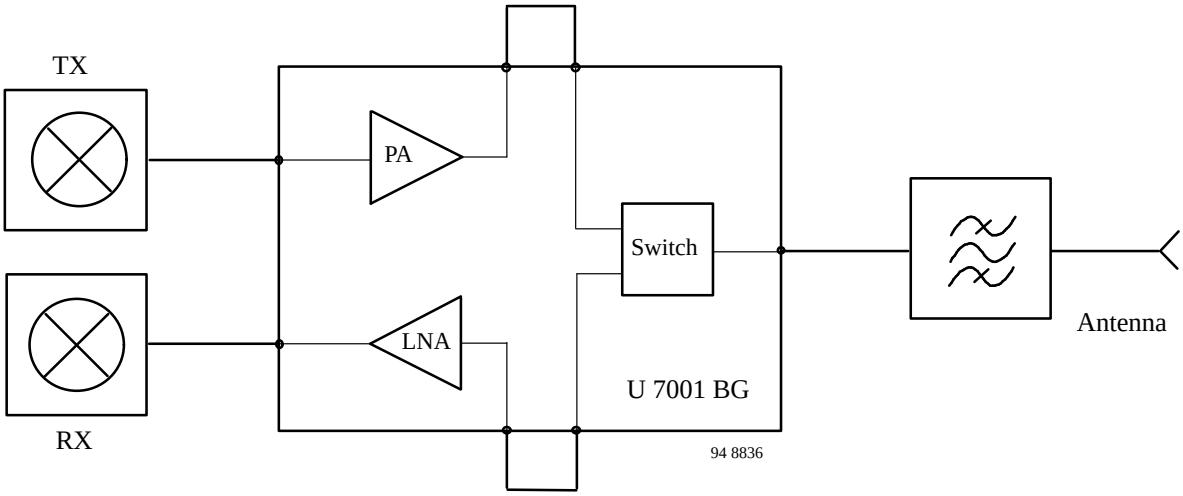

Figure 4. Application 2

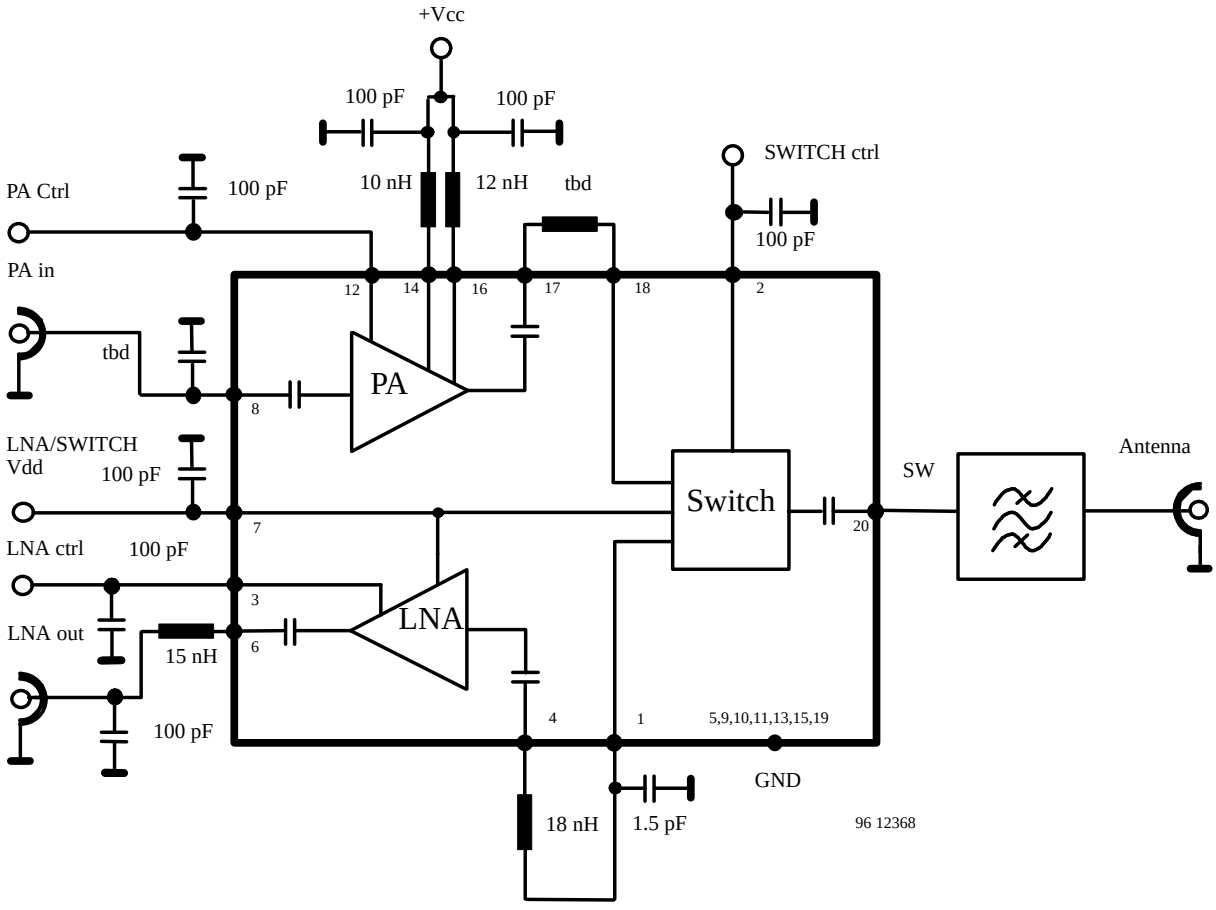

Figure 5. Application for minimal component count on FR4 board

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423